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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,208	11/19/2001	Kazuyuki Ohhashi	P21699	8111

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EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
04/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/988,208	OHHASHI, KAZUYUKI	
	Examiner	Art Unit	
	FRESHTEH N. AGHDAM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed March 2, 2009 have been fully considered but they are not persuasive.

Applicant's Argument(s):

Regarding claims 25, 26, 28, and 33, pages 5-8, the applicant argues that the claimed subject matter "amplitude adjustment after sign inversion and before phase offsetter" because (1) by performing amplitude multiplication after the first offset processing performed and before the second offset processing is performed, it is possible to reduce an amount of calculation in comparison to the prior art shown in figure 4B. (2) the applicant made the assumption that the combination of Sato and the instant application's disclosed prior art would result in the drawing shown on page 8.

Examiner's Response:

Regarding the argument set forth above, the examiner disagrees with the applicant for at least two reasons, which are as follows:

(1) The examiner is still unclear as to why the inputs to the amplitude multiplier of the admitted prior art (fig. 4B) is the same as the inputs to the amplitude multiplier of figure 4A, and as it was stated in the previous office action, Sato teaches obtaining the first phase offset of multiple of 90° using a sign inverter (means 201) and providing the second phase offset smaller than 90° using a phase offset calculation circuit to a signal output from the sign inverter (means 202). The instant application's disclosed prior art discloses adjusting the amplitude of the signal to be inputted to the phase offset

calculation circuit (fig. 4B means 406 and 407) since the inputs (SRI, SRQ) to the amplitude multiplier 406 of figure 4B (labeled as prior art) are the same as the input signals (SRI, SRQ), which are the same as the intermediate components to the amplitude multiplier of figure 4A (disclosure of the present invention), therefore, it seems that the difference between the present invention and the prior art is the way the signals SRI and SRQ are obtained not the amplitude adjustment (also see the specification, pg. 3) and, in fact, the amplitude adjuster is placed between the first phase offset processing and the second phase offset processing.

(2) In addition, one of ordinary skill in the art would recognize that amplitude adjustment and phase adjustment are necessary in the IMT2000-compliant W-CDMA (pg. 1-2) and unlike the applicant's assertion that placing the amplitude adjustment makes it possible to reduce an amount of calculation in comparison to the prior art shown in figure 4B (remarks, pages 5-6), according to the original disclosure of the invention, the invention is directed to phase offset calculation, and in particular to using two phase offset circuitries, wherein the first one is a sign inventor to obtain a first phase offset of multiple 90 degrees and the second one provides a second phase offset of smaller than 90 degrees and this two-stage configuration simplifies the circuit (e.g. reducing an amount of calculation) and reduces power consumption of the circuit (spec. pg. 1, lines 5-9; pg. 4, lines 1-28 and particularly lines 20-22; pg. 5, lines 1-5; pg. 10, lines 24-28). Therefore, the placement of the amplitude adjuster does not affect the phase adjustment, so, it would enable one of ordinary skill in the art to place the amplitude adjuster between the sign inverter and the phase offset calculation circuit,

before both the sign inverter and the phase offset calculation circuit, or after the sign inverter and the phase offset calculation circuit as long as the amplitude adjuster complies with the IMT2000 W-CDMA requirements (e.g. serves its purpose).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 32 is rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process. As to claim 32, method steps claimed in claim 32 could be mentally performed; therefore, the claimed method steps are not tied to a processor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato, further in view of the instant application's disclosed prior art.

As to claim 25, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components ; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. One of ordinary skill in the art would recognize that it is obvious and/or a matter of design choice to place the amplitude adjuster between the sign inverter and the phase offsetter in order to improve the level of the received signal as it is evidenced by the instant application's disclosed prior art (e.g. SRI and SRQ; Fig. 4B, means 406 and 407, pg. 1-2).Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught

by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

As to claim 26, Sato discloses a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. One of ordinary skill in the art would recognize that it is obvious and/or a matter of design choice to place the amplitude adjuster between the sign inverter and the phase offsetter in order to improve the level of the received signal as it is evidenced by the instant application's disclosed prior art (e.g. SRI and SRQ; Fig. 4B, means 406 and 407, pg. 1-2). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

As to claim 27, Sato further discloses that a fixed phase offset circuitry provides a predetermined amount of a fixed phase offset (Fig. 1, means 108), wherein said fixed phase offset circuitry controls a total phase offset amount with the phase offset

implemented by the sign inverter to become a desired offset amount (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claim 28, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment; and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus. One of ordinary skill in the art would recognize that it is obvious and/or a matter of design choice to place the amplitude adjuster between the sign inverter and the phase offsetter in order to improve the level of the received signal as it is evidenced by the instant application's disclosed prior art (e.g. SRI and SRQ; Fig. 4B, means 406 and 407, pg. 1-2). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver. The instant application's disclosed prior art teaches a transmission controller that provides control

information from a remote source to the phase offsetting circuit (Pg. 1, Lines 16-28; Pg. 2, Lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to control the operation of the phase offsetting circuitry based on a control signal received from a remote source as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

As to claim 29, Sato further discloses that a fixed phase offset circuitry that provides a predetermined amount of a fixed phase offset (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claims 30-31, the instant application's disclosed prior art further discloses that the phase and amplitude can be controlled for every transmit channel (Pg. 1, Lines 16-28; Pg. 2, Lines 12-20).

As to claim 32, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. One of ordinary skill in the art would recognize that it is obvious and/or a matter of design choice to place the amplitude adjuster between the sign inverter and

the phase offsetter in order to improve the level of the received signal as it is evidenced by the instant application's disclosed prior art (e.g. SRI and SRQ; Fig. 4B, means 406 and 407, pg. 1-2). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

As to claim 33, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach controlling the phase offsetting based on a signal from a remote source. The instant application's disclosed prior art teaches a transmission controller that provides control information from a remote source to the phase offsetting circuit (Pg. 1, Lines 16-28; Pg. 2, Lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to control the operation of the phase offsetting circuitry based on a control signal received from a remote source as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

As to claim 34, Sato discloses providing the sign inverted signal to phase offsetter circuitry by using at least one switch (Fig. 2, means 301).

As to claim 35, The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRESHTEH N. AGHDAM whose telephone number is (571)272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. N. A./

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611